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Principles of Verifiable RTL Design: A Functional Coding Style Supporting Verification Processes in Verilog explains how you can write Verilog to describe chip designs at the RT-level in a manner that cooperates with verification processes. This cooperation can return an order of magnitude improvement in performance and capacity from tools such as simulation and equivalence checkers. It reduces the labor costs of coverage and formal model checking by facilitating communication between the design engineer and the verification engineer. It also orients the RTL style to provide more useful results from the overall verification process. The intended audience for Principles of Verifiable RTL Design: A Functional Coding Style Supporting Verification Processes in Verilog is engineers and students who need an introduction to various design verification processes and a supporting functional Verilog RTL coding style. A second intended audience is engineers who have been through introductory training in Verilog and now want to develop good RTL writing practices for verification. A third audience is Verilog language instructors who are using a general text on Verilog as the course textbook but want to enrich their lectures with an emphasis on verification. A fourth audience is engineers with substantial Verilog experience who want to improve their Verilog practice to work better with RTL Verilog verification tools. A fifth audience is design consultants searching for proven verification-centric methodologies. A sixth audience is EDA verification tool implementers who want some suggestions about a minimal Verilog verification subset. Principles of Verifiable RTL Design: A Functional Coding Style Supporting Verification Processes in Verilog is based on the reality that comes from actual large-scale product design process and tool experience. Silicon technology now allows us to build chips consisting of tens of millions of transistors. This technology not only promises new levels of system integration onto a single chip, but also presents significant challenges to the chip designer. As a result, many ASIC developers and silicon vendors are re-examining their design methodologies, searching for ways to make effective use of the huge numbers of gates now available. These designers see current design tools and methodologies as inadequate for developing million-gate ASICs from scratch. There is considerable pressure to keep design team size and design schedules constant even as design complexities grow. Tools are not providing the productivity gains required to keep pace with the increasing gate counts available from deep submicron technology. Design reuse - the use of pre-designed and pre-verified cores - is the most promising opportunity to bridge the gap between available gate-count and designer productivity. Reuse Methodology Manual for System-On-A-Chip Designs, Second Edition outlines an effective methodology for creating reusable designs for use in a System-on-a-Chip (SoC) design methodology. Silicon and tool technologies move so quickly that no single methodology can provide a permanent solution to this highly dynamic problem. Instead, this manual is an attempt to capture and incrementally improve on current best practices in the industry, and to give a coherent, integrated view of the design process. Reuse Methodology Manual for System-On-A-Chip Designs, Second Edition will be updated on a regular basis as a result of changing technology and improved insight into the problems of design reuse and its role in producing high-quality SoC designs. In August of 2006, an engineering VP from one of Altera’s customers approached Misha Burich, VP of Engineering at Altera, asking for help in reliably being able to predict the cost, schedule and quality of system designs reliant on FPGA designs. At this time, I was responsible for defining the design flow requirements for the Altera design software and was tasked with investigating this further. As I worked with the customer to understand what worked and what did not work reliably in their FPGA design process, I noted that this problem was not unique to this one customer. The characteristics of the problem are shared by many Corporations that implement designs in FPGAs. The Corporation has many design teams at different locations and the success of the FPGA projects vary between the teams. There is a wide range of design experience across the teams. There is no working process for sharing design blocks between engineering teams. As I analyzed the data that I had received from hundreds of customer visits in the past, I noticed that design reuse among engineering teams was a challenge. I also noticed that many of the design teams at the same Companies and even within the same design team used different design methodologies. Altera had recently solved this problem as part of its own FPGA design software and IP development process. An integrated presentation of electronic circuit design and VHDL, with an emphasis on system examples and laboratory exercises. A guide to applying software design principles and coding practices to VHDL to improve the readability, maintainability, and quality of VHDL code. This book addresses an often-neglected aspect of the creation of VHDL designs. A VHDL description is also source code, and VHDL designers can use the best practices of software development to write high-quality code and to organize it in a design. This book presents this unique set of skills, teaching VHDL designers of all experience levels how to apply the best design principles and coding practices from the software world to the world of hardware. The concepts introduced here will help readers write code that is easier to understand and more likely to be correct, with improved readability, maintainability, and overall quality. After a brief review of VHDL, the book presents fundamental design principles for writing code, discussing such topics as design, quality, architecture, modularity, abstraction, and hierarchy. Building on these concepts, the book then introduces and provides recommendations for each basic element of VHDL code, including statements, design units, types, data objects, and subprograms. The book covers naming data objects and functions, commenting the source code, and visually presenting the code on the screen. All recommendations are supported by detailed rationales. Finally, the book explores two uses of VHDL: synthesis and testbenches. It examines the key characteristics of code intended for synthesis (distinguishing it from code meant for simulation) and then demonstrates the design and implementation of testbenches with a series of examples that verify different kinds of models, including combinational, sequential, and FSM code. Examples from the book are also available on a companion website, enabling the reader to experiment with the complete source code. This book presents the technical program of the International Embedded Systems Symposium (IESS) 2009. Timely topics, techniques and trends in embedded system design are covered by the chapters in this volume, including modelling, simulation, verification, test, scheduling, platforms and processors. Particular emphasis is paid to automotive systems and wireless sensor networks. Sets of actual case studies in the area of embedded system design are also included. Over recent years, embedded systems have gained an enormous amount of proce- ing power and functionality and now enter numerous application areas, due to the fact that many of the formerly external components can now be integrated into a single System-on-Chip. This tendency has resulted in a dramatic reduction in the size and cost of embedded systems. As a unique technology, the design of embedded systems is an essential element of many innovations. Embedded systems meet their performance goals, including real-time constraints, through a combination of special-purpose hardware and software components tailored to the system requirements. Both the development of new features and the reuse of existing intellectual property components are essential to keeping up with ever more demanding customer requirements. Furthermore, design complexities are steadily growing with an increasing number of components that have to cooperate properly. Embedded system designers have to cope with multiple goals and constraints simul- neously, including timing, power, reliability, dependability, maintenance, packaging and, last but not least, price. Formal methods for hardware design still find limited use in industry. Yet current practice has to change to cope with decreasing design times and increasing quality requirements. This research report presents results from the Esprit project FORMAT (formal methods in hardware verification) which involved the collaboration of the enterprises Siemens, Italtel, Telefonica I+D, TGI, and AHL, the research institute OFFIS, and the universities of Madrid and Passau. The work presented involves advanced specification languages for hardware design that are intuitive to the designer, like timing diagrams and state based languages, as well as their relation to VHDL and formal languages like temporal logic and a process-algebraic calculus. The results of experimental tests of the tools are also presented. Formal Verification: An Essential Toolkit for Modern VLSI Design presents practical approaches for design and validation, with hands-on advice to help working engineers integrate these techniques into their work. Formal Verification (FV) enables a designer to directly analyze and mathematically explore the quality or other aspects of a Register Transfer Level (RTL) design without using simulations. This can reduce time spent validating designs and more quickly reach a final design for manufacturing. Building on a basic knowledge of SystemVerilog, this book demystifies FV and presents the practical applications that are bringing it into mainstream design and validation processes at Intel and other companies. After reading this book, readers will be prepared to introduce FV in their organization and effectively deploy FV techniques to increase design and validation productivity. Learn formal verification algorithms to gain full coverage without exhaustive simulation Understand formal verification tools and how they differ from simulation tools Create instant test benches to gain insight into how models work and find initial bugs Learn from Intel insiders sharing their hard-won knowledge and solutions to complex design problems This book uses a "learn by doing" approach to introduce the concepts and techniques of VHDL and FPGA to designers through a series of hands-on experiments. FPGA Prototyping by VHDL Examples provides a collection of clear, easy-to-follow templates for quick code development; a large number of practical examples to illustrate and reinforce the concepts and design techniques; realistic projects that can be implemented and tested on a Xilinx prototyping board; and a thorough exploration of the Xilinx PicoBlaze soft-core microcontroller. The Second Edition of Writing Testbenches, Functional Verification of HDL Models presents the latest verification techniques to produce fully functional first silicon ASICs, systems-on-a-chip (SoC), boards and entire systems. From the Foreword: Building on the first edition, " ...the most successful and popular contemporary verification textbook", the author raises the verification level of abstraction by introducing coverage-driven constrained random transaction-level self-checking testbenches - all made possible through the introduction of hardware verification languages (HVLs) such as e from Verisity and OpenVera from Synopsys...." (Harry Foster, Chief Architect, Verplex Systems, Inc.) Topics included in the new Second Edition: *Discussions on OpenVera and e; *Approaches for writing constrainable random stimulus generators; *Strategies for making testbenches self-checking; *A clear blueprint of a verification process that aims for first time success; *Recent advances in functional verification such as coverage-driven verification process; *VHDL and Verilog language semantics; *The semantics are presented in new verification-oriented languages; *Techniques for applying stimulus and monitoring the response of a design; *Behavioral modeling using non-synthesizeable constructs and coding style; *Updated for Verilog 2001. VHDL Coding Styles and Methodologies was originally written as a teaching tool for a VHDL training course. The author began writing the book because he could not find a practical and easy to read book that gave in depth coverage of both, the language and coding methodologies. This book is intended for: 1. College students. It is organized in 13 chapters, each covering a separate aspect of the language, with complete examples. All VHDL code described in the book is on a companion 3.5" PC disk. Students can compile and simulate the examples to get a greater understanding of the language. Each chapter includes a series of exercises to reinforce the concepts. 2. Engineers. It is written by an aerospace engineer who has 26 years of hardware, software, computer architecture and simulation experience. It covers practical applications ofVHDL with coding styles and methodologies that represent what is current in the industry. VHDL synthesizable constructs are identified. Guidelines for testbench designs are provided. Also included is a project for the design of a synthesizable Universal Asynchronous Receiver Transmitter (UART), and a testbench to verify proper operation of the UART in a realistic environment, with CPU interfaces and transmission line jitter. An introduction to VHDL Initiative Toward ASIC Libraries (VITAL) is also provided. The book emphasizes VHDL 1987 standard but provides guidelines for features implemented in VHDL 1993. This book concentrates on common classes of hardware architectures and design problems, and focuses on the process of transitioning design requirements into synthesizable HDL code. Using his extensive, wide-ranging experience in computer architecture and hardware design, as well as in his training and consulting work, Ben provides numerous examples of real-life designs illustrated with VHDL and Verilog code. This code is shown in a way that makes it easy for the reader to gain a greater understanding of the languages and how they compare. All code presented in the book is included on the companion CD, along with other information, such as application notes. This book covers basic fundamentals of logic design and advanced RTL design concepts using VHDL. The book is organized to describe both simple and complex RTL design scenarios using VHDL. It gives practical information on the issues in ASIC prototyping using FPGAs, design challenges and how to overcome practical issues and concerns. It describes how to write an efficient RTL code using VHDL and how to improve the design performance. The design guidelines by using VHDL are also explained with the practical examples in this book. The book also covers the ALTERA and XILINX FPGA architecture and the design flow for the PLDs. The contents of this book will be useful to students, researchers, and professionals working in hardware design and optimization. The book can also be used as a text for graduate and professional development courses. Compendio de los trabajos presentados en Toledo durante el VHDL user's forum in Europe. VHDL Coding Styles and Methodologies, Edition is a follow up book to the first edition of same book and to VHDL Answers to Frequently Asked Questions, first and second editions. This book was originally written as a teaching tool for a VHDL training course. The author began writing the book because he could not find a practical and easy to read book that gave in depth coverage of both, the language and coding methodologies. This edition provides practical information on reusable software methodologies for the design of bus functional models for testbenches. It also provides guidelines in the use of VHDL for synthesis. All VHDL code described in the book is on a companion CD. The CD also includes the GNU toolsuite with EMACS language sensitive editor (with VHDL, Verilog, and other language templates), and TSHELL tools that emulate a Unix shell. Model Technology graciously included a timed evaluation version of ModelSim, a recognized industry standard VHDL/Verilog compiler and simulator that supports easy viewing of the models under analysis, along with many debug features. In addition, Synplicity included a timed version of Synplify, a very efficient, user friendly and easy to use FPGA synthesis tool. Synplify provides a user both the RTL and gate level views of the synthesized model, and a performance report of the design. Optimization mechanisms are provided in the tool. CHAPTER 6 Architecting Testbenches 221 Reusable Verification Components 221 Procedural Interface 225 Development Process 226 Verilog Implementation 227 Packaging Bus-Functional Models 228 Utility Packages 231 VHDL Implementation 237 Packaging Bus-Functional Procedures 238 240 Creating a Test Harness 243 Abstracting the Client/Server Protocol Managing Control Signals 246 Multiple Server Instances 247 Utility Packages 249 Autonomous Generation and Monitoring 250 Autonomous Stimulus 250 Random Stimulus 253 Injecting Errors 255 Autonomous Monitoring 255 258 Autonomous Error Detection Input and Output Paths 258 Programmable Testbenches 259 Configuration Files 260 Concurrent Simulations 261 Compile-Time Configuration 262 Verifying Configurable Designs 263 Configurable Testbenches 265 Top Level Generics and Parameters 266 Summary 268 CHAPTER 7 Simulation Management 269 Behavioral Models 269 Behavioral versus Synthesizable Models 270 Example of Behavioral Modeling 271 Characteristics of a Behavioral Model 273 x Writing Testbenches: Functional Verification of HDL Models Modeling Reset 276 Writing Good Behavioral Models

281 Behavioral Models Are Faster 285 The Cost of Behavioral Models 286 The Benefits of Behavioral Models 286 Demonstrating Equivalence 289 Pass or Fail? 289 Managing Simulations 292 294 Configuration Management Verilog Configuration Management 295 VHDL Configuration Management 301 SDF Back-Annotation 305 Output File Management 309 Regression 312 Running Regressions 313 Regression Management 314 Summary 316 APPENDIX A Coding Guidelines 317 Directory Structure 318 VHDL Specific 320 Verilog Specific 320 General Coding Guidelines 321 Comments 321 Layout 323 Syntax 326 Debugging 329 Naming Guidelines 329 Capitalization 330 Identifiers 332 Constants 334 334 HDL Specific Filenames 336 HDL Coding Guidelines 336 337 Structure 337 Layout Logic synthesis has become a fundamental component of the ASIC design flow, and Logic Synthesis Using Synopsys® has been written for all those who dislike reading manuals but who still like to learn logic synthesis as practised in the real world. The primary focus of the book is Synopsys Design Compiler®: the leading synthesis tool in the EDA marketplace. The book is specially organized to assist designers accustomed to schematic capture based design to develop the required expertise to effectively use the Compiler. Over 100 `classic scenarios' faced by designers using the Design Compiler have been captured and discussed, and solutions provided. The scenarios are based both on personal experiences and actual user queries. A general understanding of the problem-solving techniques provided will help the reader debug similar and more complicated problems. Furthermore, several examples and dc-shell scripts are provided. Specifically, Logic Synthesis Using Synopsys® will help the reader develop a better understanding of the synthesis design flow, optimization strategies using the Design Compiler, test insertion using the Test Compiler®, commonly used interface formats such as EDIF and SDF, and design re-use in a synthesis-based design methodology. Examples have been provided in both VHDL and Verilog. Audience: Written with CAD engineers in mind to enable them to formulate an effective synthesis-based ASIC design methodology. Will also assist design teams to better incorporate and effectively integrate synthesis with their existing in-house design methodology and CAD tools. This book offers readers a set of new approaches and tools a set of tools and techniques for facing challenges in parallelization with design of embedded systems. It provides an advanced parallel simulation infrastructure for efficient and effective system-level model validation and development so as to build better products in less time. Since parallel discrete event simulation (PDES) has the potential to exploit the underlying parallel computational capability in today’s multi-core simulation hosts, the author begins by reviewing the parallelization of discrete event simulation, identifying problems and solutions. She then describes out-of-order parallel discrete event simulation (OoO PDES), a novel approach for efficient validation of system-level designs by aggressively exploiting the parallel capabilities of todays’ multi-core PCs. This approach enables readers to design simulators that can fully exploit the parallel processing capability of the multi-core system to achieve fast speed simulation, without loss of simulation and timing accuracy. Based on this parallel simulation infrastructure, the author further describes automatic approaches that help the designer quickly to narrow down the debugging targets in faulty ESL models with parallelism. Reuse Techniques for VLSI Design is a reflection on the current state of the art in design reuse for microelectronic systems. To that end, it is the first book to garner the input of leading experts from both research and application areas. These experts document herein not only their more mature approaches, but also their latest research results. Firstly, it sets out the background and support from international organisations that enforce System-on-a-Chip (SoC) design by reuse- oriented methodologies. This overview is followed by a number of technical presentations covering different requirements of the reuse domain. These are presented from different points of view, i.e., IP provider, IP user, designer, isolated reuse, intra-company or inter-company reuse. More general systems or case studies, e.g., metrics, are followed by comprehensive reuse systems, e.g., reuse management systems partly including business models. Since design reuse must not be restricted to digital components, mixed- signal and analog reuse approaches are also presented. In parallel to the digital domain, this area covers research in reuse database design. Design verification and legal aspects are two important topics that are closely related to the realization of design reuse. These hot topics are covered by presentations that finalize the survey of outstanding research, development and application of design reuse for SoC design. Reuse Techniques for VLSI Design is an invaluable reference for researchers and engineers involved in VLSI/ASIC design. The analysis was performed by designing and implementing a screensaver circuit on an FPGA and displaying it on the VGA Monitor. This practical, tool-independent guide to designing digital circuits takes a unique, top-down approach, reflecting the nature of the design process in industry. Starting with architecture design, the book comprehensively explains the why and how of digital circuit design, using the physics designers need to know, and no more. The time has come for high-level synthesis. When research into synthesizing hardware from abstract, program-like de scriptions started in the early 1970' s, there was no automated path from the register transfer design produced by high-level synthesis to a complete hardware imple mentation. As a result, it was very difficult to measure the effectiveness of high level synthesis methods; it was also hard to justify to users the need to automate architecture design when low-level design had to be completed manually. Today's more mature CAD techniques help close the gap between an automat ically synthesized design and a manufacturable design. Market pressures encour age designers to make use of any and all automated tools. Layout synthesis, logic synthesis, and specialized datapath generators make it feasible to quickly imple ment a register-transfer design in silicon,leaving designers more time to consider architectural improvements. As IC design becomes more automated, customers are increasing their demands; today's leading edge designers using logic synthesis systems are training themselves to be tomorrow's consumers of high-level synthe sis systems. The need for very fast turnaround, a competitive fabrication market WhlCh makes small-quantity ASIC manufacturing possible, and the ever growing co:n plexity of the systems being designed, all make higher-level design automaton inevitable. The push to move products to market as quickly and cheaply as possible is fiercer than ever, and accordingly, engineers are always looking for new ways to provide their companies with the edge over the competition. Field-Programmable Gate Arrays (FPGAs), which are faster, denser, and more cost-effective than traditional programmable logic devices (PLDs), are quickly becoming one of the most widespread tools that embedded engineers can utilize in order to gain that needed edge. FPGAs are especially popular for prototyping designs, due to their superior speed and efficiency. This book hones in on that rapid prototyping aspect of FPGA use, showing designers exactly how they can cut time off production cycles and save their companies money drained by costly mistakes, via prototyping designs with FPGAs first. Reading it will take a designer with a basic knowledge of implementing FPGAs to the “next-level of FPGA use because unlike broad beginner books on FPGAs, this book presents the required design skills in a focused, practical, example-oriented manner. In-the-trenches expert authors assure the most applicable advice to practicing engineers Dual focus on successfully making critical decisions and avoiding common pitfalls appeals to engineers pressured for speed and perfection Hardware and software are both covered, in order to address the growing trend toward "cross-pollination" of engineering expertise This book shares with readers practical design knowledge gained from the author’s 24 years of IC design experience. The author addresses issues and challenges faced commonly by IC designers, along with solutions and workarounds. Guidelines are described for tackling issues such as clock domain crossing, using lockup latch to cross clock domains during scan shift, implementation of scan chains across power domain, optimization methods to improve timing, how standard cell libraries can aid in synthesis optimization, BKM (best known method) for RTL coding, test compression, memory BIST, usage of signed Verilog for design requiring +ve and -ve calculations, state machine, code coverage and much more. Numerous figures and examples are provided to aid the reader in understanding the issues and their workarounds. The skills and guidance needed to master RTL hardware design This book teaches readers how to systematically design efficient,portable, and scalable Register Transfer Level (RTL) digitalcircuits using the VHDL hardware description language and synthesissoftware. Focusing on the module-level design, which is composed offunctional units, routing circuit, and storage, the bookillustrates the relationship between the VHDL constructs and theunderlying hardware components, and shows how to develop codes thatfaithfully reflect the module-level design and can be synthesizedinto efficient gate-level implementation. Several unique features distinguish the book: * Coding style that shows a clear relationship between VHDLconstructs and hardware components * Conceptual diagrams that illustrate the realization of VHDLcodes * Emphasis on the code reuse * Practical examples that demonstrate and reinforce designconcepts, procedures, and techniques * Two chapters on realizing sequential algorithms in hardware * Two chapters on scalable and parameterized designs andcoding * One chapter covering the synchronization and interface betweenmultiple clock domains Although the focus of the book is RTL synthesis, it also examinesthe synthesis task from the perspective of the overall developmentprocess. Readers learn good design practices and guidelines toensure that an RTL design can accommodate future simulation,verification, and testing needs, and can be easily incorporatedinto a larger system or reused. Discussion is independent oftechnology and can be applied to both ASIC and FPGA devices. With a balanced presentation of fundamentals and practicalexamples, this is an excellent textbook for upper-levelundergraduate or graduate courses in advanced digital logic.Engineers who need to make effective use of today's synthesissoftware and FPGA devices should also refer to this book. This textbook for courses in Embedded Systems introduces students to necessary concepts, through a hands-on approach. It gives a great introduction to FPGA-based microprocessor system design using state-of-the-art boards, tools, and microprocessors from Altera/Intel® and Xilinx®. HDL-based designs (soft-core), parameterized cores (Nios II and MicroBlaze), and ARM Cortex-A9 design are discussed, compared and explored using many hand-on designs projects. Custom IP for HDMI coder, Floating-point operations, and FFT bit-swap are developed, implemented, tested and speed-up is measured. Downloadable files include all design examples such as basic processor synthesizable code for Xilinx and Altera tools for PicoBlaze, MicroBlaze, Nios II and ARMv7 architectures in VHDL and Verilog code, as well as the custom IP projects. Each Chapter has a substantial number of short quiz questions, exercises, and challenging projects. Explains soft, parameterized, and hard core systems design tradeoffs; Demonstrates design of popular KCPSM6 8 Bit microprocessor step-by-step; Discusses the 32 Bit ARM Cortex-A9 and a basic processor is synthesized; Covers design flows for both FPGA Market leaders Nios II Altera/Intel and MicroBlaze Xilinx system; Describes Compiler-Compiler Tool development; Includes a substantial number of Homework’s and FPGA exercises and design projects in each chapter. This book describes best practices for successful FPGA design. It is the result of the author’s meetings with hundreds of customers on the challenges facing each of their FPGA design teams. By gaining an understanding into their design environments, processes, what works and what does not work, key areas of concern in implementing system designs have been identified and a recommended design methodology to overcome these challenges has been developed. This book’s content has a strong focus on design teams that are spread across sites. The goal being to increase the productivity of FPGA design teams by establishing a common methodology across design teams; enabling the exchange of design blocks across teams. Coverage includes the complete FPGA design flow, from the basics to advanced techniques. This new edition has been enhanced to include new sections on System modeling, embedded design and high level design. The original sections on Design Environment, RTL design and timing closure have all been expanded to include more up to date techniques as well as providing more extensive scripts and RTL code that can be reused by readers. Presents complete, field-tested methodology for FPGA design, focused on reuse across design teams; Offers best practices for FPGA timing closure, in-system debug, and board design; Details techniques to resolve common pitfalls in designing with FPGAs. Use Arrow's affordable and breadboard-friendly FPGA development board (BeMicro MAX 10) to create a light sensor, temperature sensor, motion sensor, and the KITT car display from Knight Rider. You don't need an electronics engineering degree or even any programming experience to get the most out of Beginning FPGA: Programming Metal. Just bring your curiosity and your Field-Programmable Gate Array. This book is for those who have tinkered with Arduino or Raspberry Pi, and want to get more hands-on experience with hardware or for those new to electronics who just want to dive in. You'll learn the theory behind FPGAs and electronics, including the math and logic you need to understand what's happening - all explained in a fun, friendly, and accessible way. It also doesn't hurt that you'll be learning VHDL, a hardware description language that is also an extremely marketable skill. What You'll Learn: Learn what an FPGA is and how it's different from a microcontroller or ASIC Set up your toolchain Use VHDL, a popular hardware description language, to tell your FPGA what to be Explore the theory behind FPGA and electronics Use your FPGA with a variety of sensors and to talk to a Raspberry Pi Who This Book is For: Arduino, Raspberry Pi, and other electronics enthusiasts who want a clear and practical introduction to FPGA. Compendio de los trabajos presentados en Toledo durante el 2nd Workshop on Libraries, component modeling and quality assurance. Design reuse is not just a topic of research but a real industrial necessity in the microelectronic domain and thus driving the competitiveness of relevant areas like for example telecommunication or automotive. Most companies have already dedicated a department or a central unit that transfer design reuse into reality. All main EDA conferences include a track to the topic, and even specific conferences have been established in this area, both in the USA and in Europe. Virtual Components Design and Reuse presents a selection of articles giving a mature and consolidated perspective to design reuse from different points of view. The authors stem from all relevant areas: research and academia, IP providers, EDA vendors and industry. Some classical topics in design reuse, like specification and generation of components, IP retrieval and cataloguing or interface customisation, are revisited and discussed in depth. Moreover, new hot topics are presented, among them IP quality, platform-based reuse, software IP, IP security, business models for design reuse, and major initiatives like the MEDEA EDA Roadmap. This book constitutes the refereed proceedings of the 4th International Workshop on Systems, Architectures, Modeling, and Simulation, SAMOS 2004, held in Samos, Greece on July 2004. Besides the SAMOS 2004 proceedings, the book also presents 19 revised papers from the predecessor workshop SAMOS 2003. The 55 revised full papers presented were carefully reviewed and selected for inclusion in the book. The papers are organized in topical sections on reconfigurable computing, architectures and implementation, and systems modeling and simulation. A presentation of circuit synthesis and circuit simulation using VHDL (including VHDL 2008), with an emphasis on design examples and laboratory exercises. This text offers a comprehensive treatment of VHDL and its applications to the design and simulation of real, industry-standard circuits. It focuses on the use of VHDL rather than solely on the language, showing why and how certain types of circuits are inferred from the language constructs and how any of the four simulation categories can be implemented. It makes a rigorous distinction between VHDL for synthesis and VHDL for simulation. The VHDL codes in all design examples are complete, and circuit diagrams, physical synthesis in FPGAs, simulation results, and explanatory comments are included with the designs. The text reviews fundamental concepts of digital electronics and design and includes a series of appendixes that offer tutorials on important design tools including ISE, Quartus II, and ModelSim, as well as descriptions of programmable logic devices in which the designs are implemented, the DE2 development board, standard VHDL packages, and other features. All four VHDL editions (1987, 1993, 2002, and 2008) are covered. This expanded second edition is the first textbook on VHDL to include a detailed analysis of circuit simulation with VHDL testbenches in all four categories (nonautomated, fully automated, functional, and timing simulations), accompanied by complete practical examples. Chapters 1–9 have been updated, with new design examples and new details on such topics as data types and code statements. Chapter 10 is entirely new and deals exclusively with simulation. Chapters 11–17 are also entirely new, presenting extended and advanced designs with theoretical and practical coverage of serial data communications circuits, video circuits, and other topics. There are many more illustrations, and the exercises have been updated and their number more than doubled. A guide to applying software design principles and coding practices to VHDL to improve the readability, maintainability, and quality of VHDL code. This book addresses an often-neglected aspect of the creation of VHDL designs. A VHDL description is also source code, and VHDL designers can use the best practices of software development to write high-quality code and to organize it in a design. This book presents this unique set of skills, teaching VHDL designers of all experience levels how to apply the best design principles and coding practices from the software world to the world of hardware. The concepts introduced here will help readers write code that is easier to understand and more likely to be correct, with improved readability, maintainability, and overall quality. After a brief review of VHDL, the book presents fundamental design principles for writing code, discussing such topics as design, quality, architecture, modularity, abstraction, and hierarchy. Building on these concepts, the book then introduces and provides recommendations for each basic element of VHDL code, including statements, design units, types, data objects, and subprograms. The book covers naming data objects and functions, commenting the source code, and visually presenting the code on the screen. All recommendations are supported by detailed rationales. Finally, the book explores two uses of VHDL: synthesis and testbenches. It examines the key characteristics of code intended for synthesis (distinguishing it from code meant for simulation) and then demonstrates the design and implementation of testbenches with a series of examples that verify different kinds of models, including combinational, sequential, and FSM code. Examples from the book are also available on a companion website, enabling the reader to experiment with the complete source code. Provides students with a system-level perspective and the tools they need to understand, analyze and design complete digital systems using VHDL. It goes beyond the design of simple combinational and sequential modules to show how such modules are used to build complete systems, reflecting digital design in the real world. mental improvements during the same period. What is clearly needed in verification techniques and technology is the equivalent of a synthesis productivity breakthrough. In

the second edition of Writing Testbenches, Bergeron raises the verification level of abstraction by introducing coverage-driven constrained-random transaction-level self-checking testbenches all made possible through the introduction of hardware verification languages (HVLs), such as e from Verisity and OpenVera from Synopsys. The state-of-art methodologies described in Writing Test benches will contribute greatly to the much-needed equivalent of a synthesis breakthrough in verification productivity. I not only highly recommend this book, but also I think it should be required reading by anyone involved in design and verification of today's ASIC, SoCs and systems. Harry Foster Chief Architect Verplex Systems, Inc. xviii Writing Testbenches: Functional Verification of HDL Models PREFACE If you survey hardware design groups, you will learn that between 60% and 80% of their effort is now dedicated to verification. Artificial Intelligence in Economics and Managemetn to Requirements Engineering VHDL Answers to Frequently asked Questions is a follow-up to the author's book VHDL Coding Styles and Methodologies (ISBN 0-7923-9598-0). On completion of his first book, the author continued teaching VHDL and actively participated in the comp. lang. vhdl newsgroup. During his experiences, he was enlightened by the many interesting issues and questions relating to VHDL and synthesis. These pertained to: misinterpretations in the use of the language; methods for writing error free, and simulation efficient, code for testbench designs and for synthesis; and general principles and guidelines for design verification. As a result of this wealth of public knowledge contributed by a large VHDL community, the author decided to act as a facilitator of this information by collecting different classes of VHDL issues, and by elaborating on these topics through complete simulatable examples. This book is intended for those who are seeking an enhanced proficiency in VHDL. Its target audience includes: 1. Engineers. The book addresses a set of problems commonly experienced by real users of VHDL. It provides practical explanations to the questions, and suggests practical solutions to the raised issues. It also includes packages to achieve common utilities, useful in the generation of debug code aDd testbench designs. These packages include conversions to strings (the IMAGE package), generation of Linear Feedback Shift Registers (LFSR), Multiple Input Shift Register (MISR), and random number generators. This revised and updated third edition outlines a set of best practices for creating reusable designs for use in an System-on-a-Chip (SoC) design methodology. These practices are based on the authors' experience in developing reusable designs, as well as the experience of design teams in many companies around the world. Software quality is a generalised statement difficult to agree or disagree with until a precise definition of the concept of "Software Quality" is reached in terms of measurable quantities. Unfortunately, for the software technology the basic question of: • what to measure; • how to measure; • when to measure; • how to deal with the data obtained are still unanswered and are also closely dependant on the field of application. In the past twenty years or more there have been a number of conferences and debates focusing on the concept of Software Quality, which produced no real industrial impact. Recently, however, the implementation of a few generic standards (ISO 9000, IEEE etc.) has produced and improved application of good practice principles at the industrial level. As a graduate in PhYSiCS, I still believe it is a long way before the concept of Software Quality can be defined exactly and measured, if ever. This is way I think the AQuIS series of conferences is important, its object begin to provide a platform for the transfer of technology and know how between Academic, Industrial and Research Institutions, in the field of Software Quality. Their objects are: • to provide a forum for the introduction and discussion of new research breakthroughs in Software Quality; • to provide professional Software Quality engineers with the necessary exposure to the results of current research; • to expose the research community to the problems of practical application of new results.

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